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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/809,374	03/26/2004	Munehiro Uratani	1248-0709PUS1	7619

2292 7590 02/21/2008

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EXAMINER	
LEE, SIU M	

ART UNIT	PAPER NUMBER
2611	

NOTIFICATION DATE	DELIVERY MODE
02/21/2008	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

mailroom@bskb.com

Office Action Summary	Application No.	Applicant(s)	
	10/809,374	URATANI ET AL.	
	Examiner	Art Unit	
	Siu M. Lee	2611	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *09 November 2007*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-7 and 9* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *9* is/are rejected.

7)☒ Claim(s) *1-7* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *26 March 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

1. Applicant's arguments, see page 8, filed 11/9/2007, with respect to rejection of claims under 35 U.S.C. §103 have been fully considered and are persuasive. The 35 U.S.C. §103 rejection of claim 1, 2, 4-6 has been withdrawn.

Claim Objections

2. Claims 1-7 are objected to because of the following informalities:

(1) Regarding claim 1:

Line 3 recites "a voltage selecting section for selecting, from the plurality of adjustment voltage, an adjustment voltage that is in accordance with a delay time adjustment amount which is set so that delay time of each block in an integrated circuit becomes closer to an average value of the delay time, the delay time being time between an input of data to the circuit block". According to figure 6 of the instant application, an adjustment voltage for each circuit block is selected by the selector 12. The examiner suggest to change the above quoted paragraph to ---**a voltage selecting section for selecting, from the plurality of adjustment voltage, an adjustment voltage for each circuit block that is in accordance with a delay time adjustment amount which is set so that delay time of each block in an integrated circuit becomes closer to an average value of the delay time of all circuit blocks, the delay time being time between an input of data to a circuit block**--- for clarification.

Also, in line 8-10, the examiner suggest to change "a delay-adjustment section for increasing or decreasing the delay time by using a transistor at which a threshold voltage changes in accordance with a value of the adjustment voltage selected." to --- **a delay-adjustment section for increasing or decreasing the delay time of each circuit block by using transistors at which a threshold voltages change in accordance with values of the adjustment voltage selected.**--- for clarification.

(2) Regarding claim 3:

Lines 4 recites "a voltage selecting section for selecting, from the plurality of adjustment voltages, an adjustment voltage that is in accordance with a delay time adjustment amount which is set so that delay time of each block in an integrated circuit becomes closer to an average value of the delay time, the delay time being time between an input of data to the circuit block". According to figure 6 of the instant application, an adjustment voltage for each circuit block is selected by the selector 12. The examiner suggest to change the above quoted paragraph to ---**a voltage selecting section for selecting, from the plurality of adjustment voltages, an adjustment voltage for each circuit block that is in accordance with a delay time adjustment amount which is set so that delay time of each block in an integrated circuit becomes closer to an average value of the delay time of all circuit blocks, the delay time being time between an input of data to a circuit block**--- for clarification.

Also, in line 9-11, the examiner suggest to change "a delay-adjustment section for increasing or decreasing the delay time by using a transistor at which a threshold voltage changes in accordance with a value of the adjustment voltage selected." to --- **a**

delay-adjustment section for increasing or decreasing the delay time of each circuit block by using transistors at which a threshold voltages change in accordance with values of the adjustment voltage selected.--- for clarification.

(3) Regarding claim 7:

Line 5 recites "a voltage selecting section for selecting, from the plurality of adjustment voltage, an adjustment voltage that is in accordance with a delay time adjustment amount which is set so that delay time of each block in an integrated circuit becomes closer to an average value of the delay time, the delay time being time between an input of data to the circuit block". According to figure 6 of the instant application, an adjustment voltage for each circuit block is selected by the selector 12. The examiner suggest to change the above quoted paragraph to ---**a voltage selecting section for selecting, from the plurality of adjustment voltage, an adjustment voltage for each circuit block that is in accordance with a delay time adjustment amount which is set so that delay time of each block in an integrated circuit becomes closer to an average value of the delay time of all circuit blocks, the delay time being time between an input of data to a circuit block**--- for clarification.

Also, in line 11-13 the examiner suggest to change "a delay-adjustment section for increasing or decreasing the delay time by using a transistor at which a threshold voltage changes in accordance with a value of the adjustment voltage selected." to --- **a delay-adjustment section for increasing or decreasing the delay time of each circuit block by using transistors at which a threshold voltages change in accordance with values of the adjustment voltage selected.**--- for clarification.

Appropriate correction is required.

Claim Rejections - 35 USC § 112

3. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

4. Claim 9 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 9 is directed to a computer-readable storage medium storing a signal timing adjustment amount setting program for a signal timing adjustment system. The claim recites that the computer-readable storage medium including a signal timing adjustment section, a delay measurement section, an average value calculating section, and an adjustment amount setting section. It is not possible for a computer-readable storage medium to include all these section and perform the functions of all these sections. It is unclear whether the claim is directed to a computer-readable storage medium or the sections (a signal timing adjustment section, a delay measurement section, an average value calculating section, and an adjustment amount setting section).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Siu M. Lee whose telephone number is (571) 270-1083.

The examiner can normally be reached on Mon-Fri, 7:30-4:00 with every other Friday off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Chieh Fan can be reached on (571) 272-3042. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Siu M Lee
Examiner
Art Unit 2611
2/7/2008

CHIEH M. FAN
SUPERVISORY PATENT EXAMINER